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Rombach

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(54) **HIGH SPEED, RAIL-TO-RAIL CMOS DIFFERENTIAL INPUT STAGE**

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(51) **Int. Cl.**

H03F 3/45	(2006.01)
H03F 1/02	(2006.01)
H03F 3/30	(2006.01)

(52) **U.S. Cl.**

CPC ***H03F 3/45237*** (2013.01); ***H03F 1/0205*** (2013.01); ***H03F 1/0233*** (2013.01); ***H03F 3/3022*** (2013.01); ***H03F 3/45076*** (2013.01); ***H03F 3/45183*** (2013.01); *H03F 2200/129* (2013.01); *H03F 2200/453* (2013.01); *H03F 2200/513* (2013.01); *H03F 2203/45066* (2013.01); *H03F 2203/45116* (2013.01)

(58) **Field of Classification Search**

CPC H03F 1/0233; H03F 3/45076; H03F 2200/129; H03F 2203/45066; H03F 2203/45116

See application file for complete search history.

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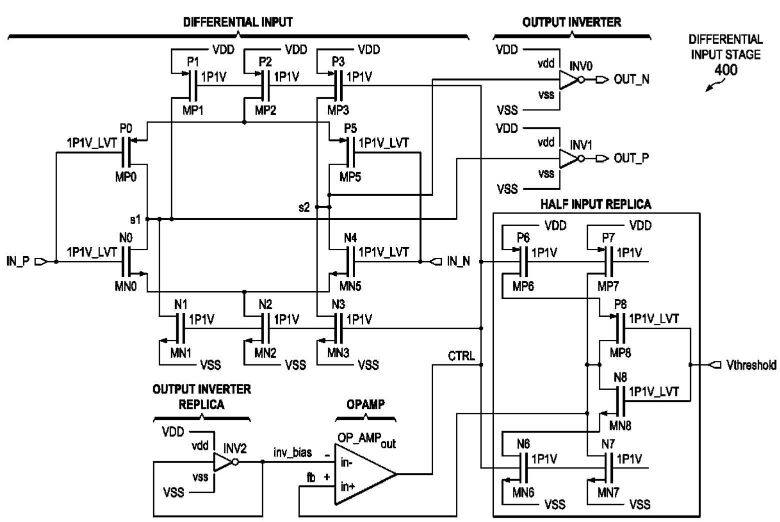
(57) **ABSTRACT**

An apparatus is provided, comprising a single-ended input stage with signals IN_P & IN_N as input and OUT_P & OUT_N as output, wherein the differential input controlled by transistors P**1**-**3** and N**1**-N**3**; and a means for weighting (sizing) of transistor (P**1** & P**3**) relative to P**2** and (N**1** & N**3**) relative to N**2** defines the optimal operation mode.

5 Claims, 11 Drawing Sheets



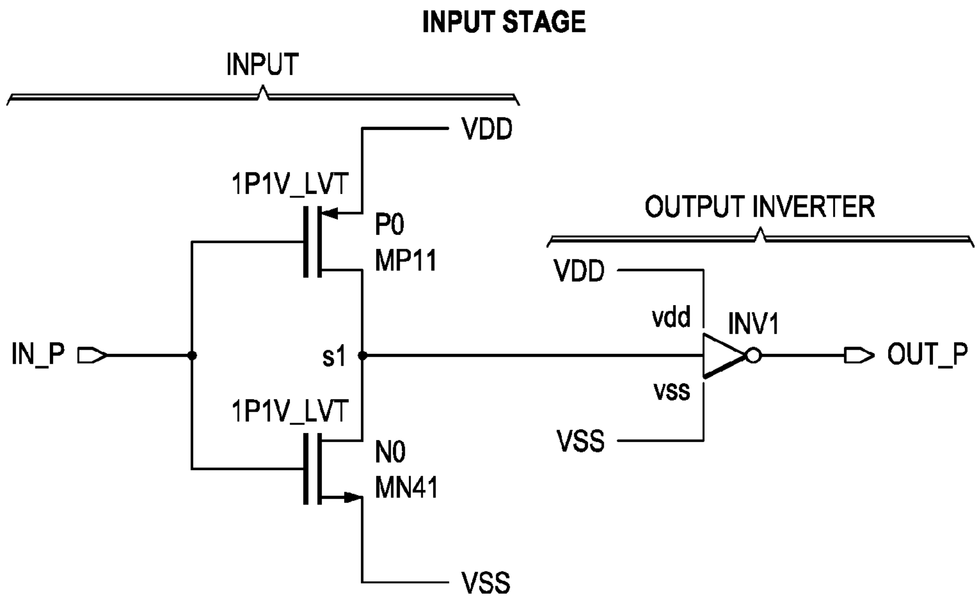


FIG. 1
(PRIOR ART)

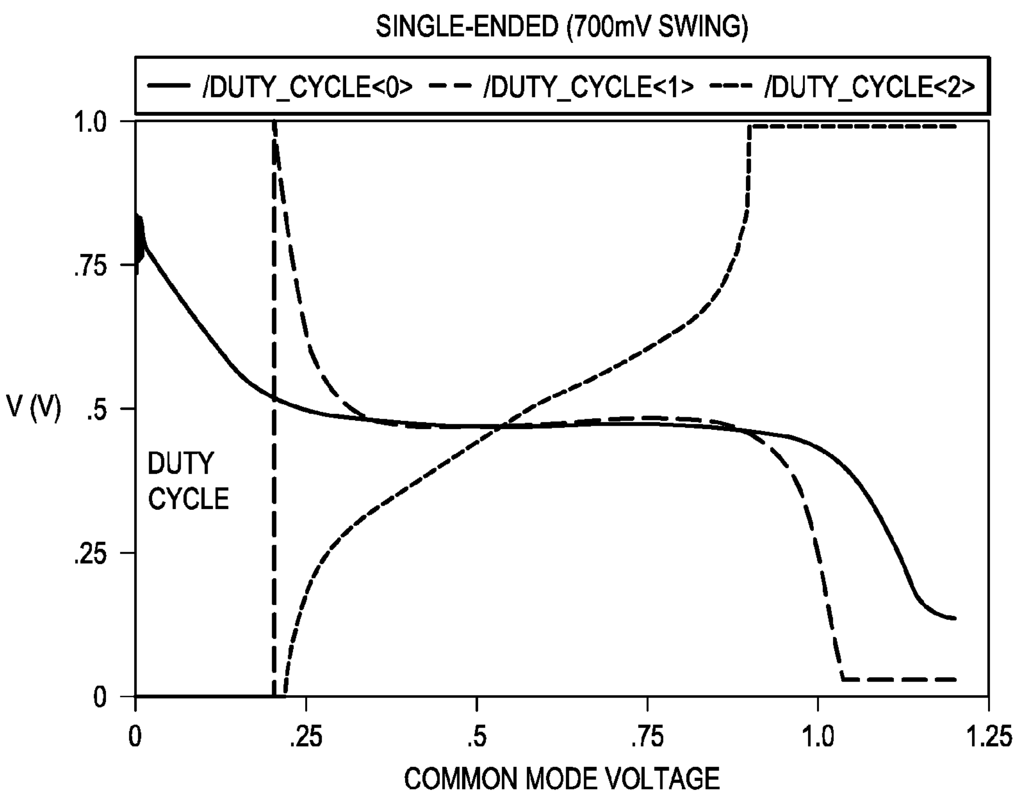
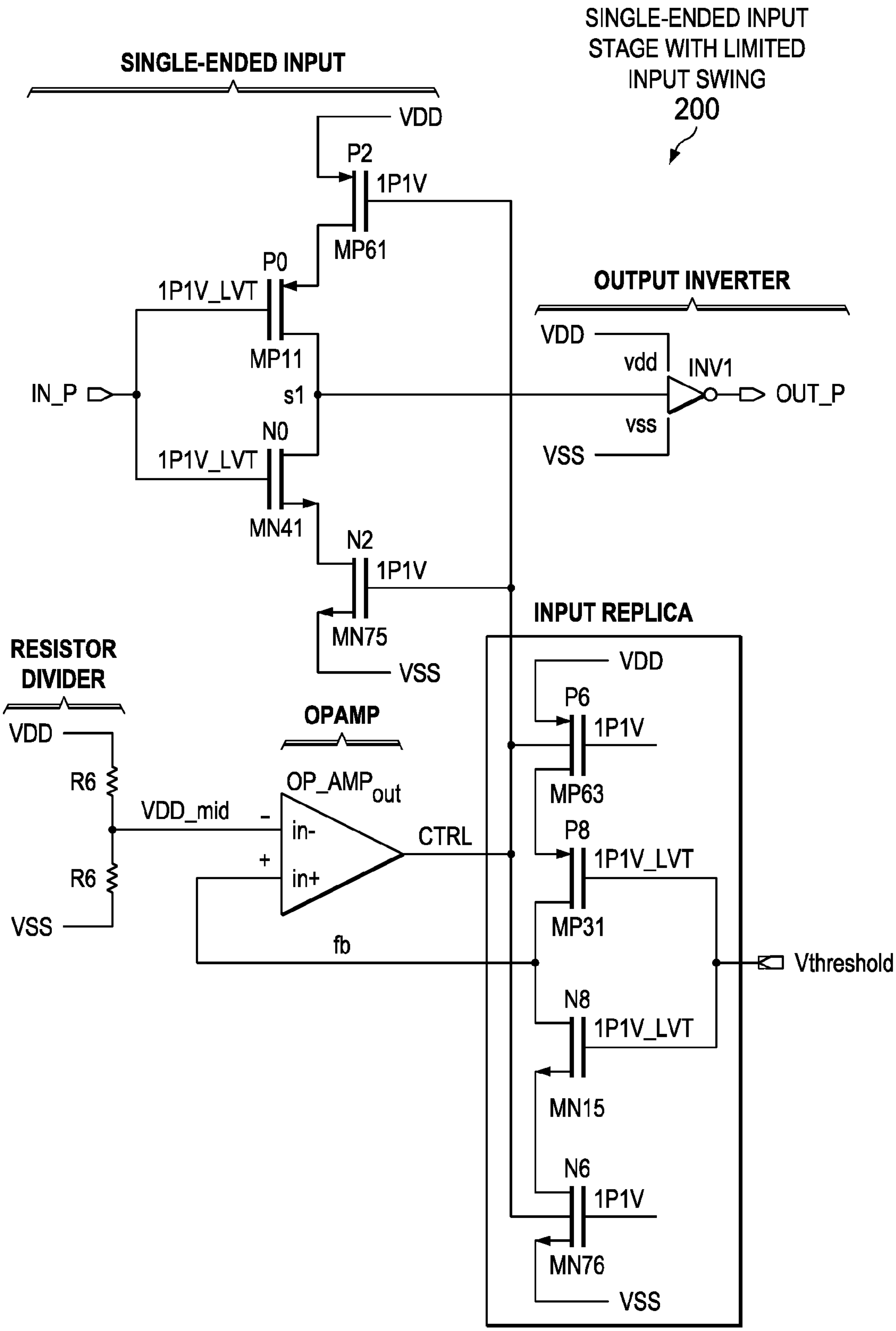


FIG. 7I



SINGLE-ENDED INPUT STAGE WITH LIMITED INPUT SWING
200
SINGLE-ENDED INPUT
VDD
P2
1P1V
MP61
P0
1P1V_LVT
MP11
IN_P
s1
N0
1P1V_LVT
MN41
N2
1P1V
MN75
VSS
OUTPUT INVERTER
VDD
vdd
INV1
OUT_P
vss
VSS
INPUT REPLICA
VDD
P6
1P1V
MP63
P8
1P1V_LVT
MP31
Vthreshold
N8
1P1V_LVT
MN15
N6
1P1V
MN76
VSS
RESISTOR DIVIDER
VDD
R6
VDD_mid
R6
VSS
OPAMP
OP_AMPout
in-
in+
CTRL
fb

FIG. 2A

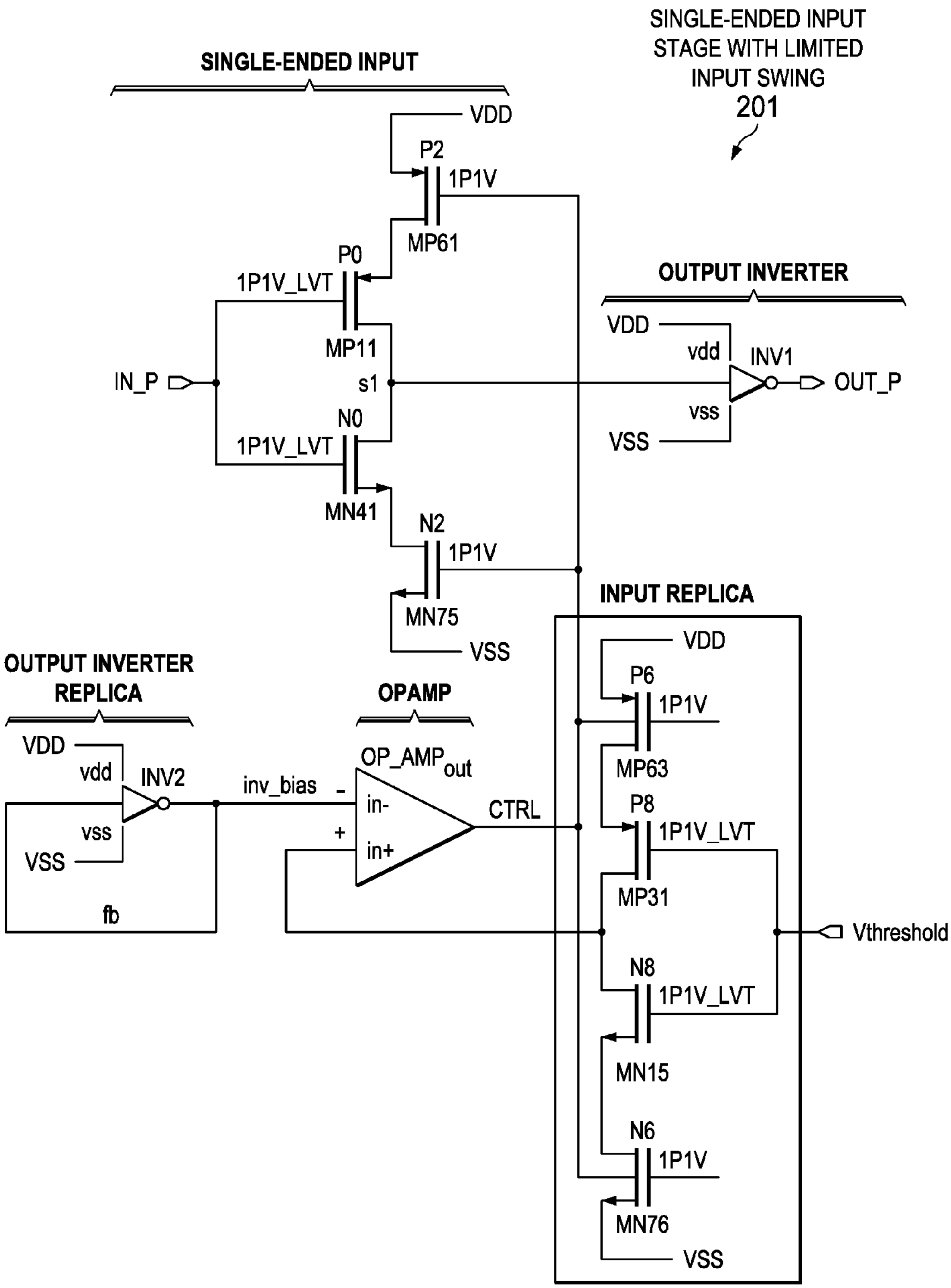

SINGLE-ENDED INPUT STAGE WITH LIMITED INPUT SWING
201
SINGLE-ENDED INPUT
VDD
P2
1P1V
MP61
P0
1P1V_LVT
MP11
IN_P
s1
N0
1P1V_LVT
MN41
N2
1P1V
MN75
VSS
OUTPUT INVERTER
VDD
vdd
INV1
OUT_P
vss
VSS
INPUT REPLICA
VDD
P6
1P1V
MP63
P8
1P1V_LVT
MP31
Vthreshold
N8
1P1V_LVT
MN15
N6
1P1V
MN76
VSS
OUTPUT INVERTER REPLICA
VDD
vdd
INV2
vss
VSS
fb
OPAMP
OP_AMP out
inv_bias
-
in-
+
in+
CTRL

FIG. 2B

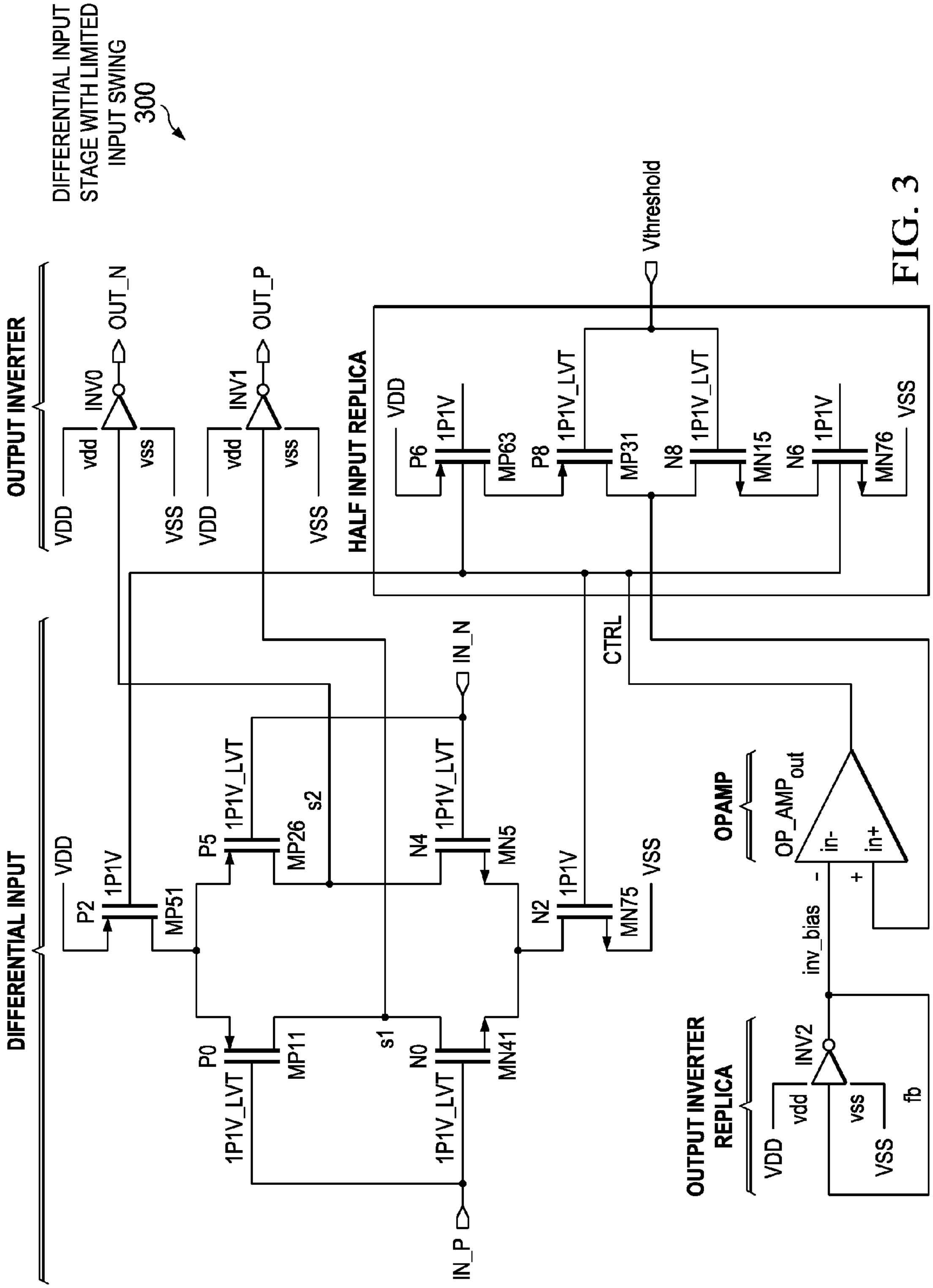

DIFFERENTIAL INPUT STAGE WITH LIMITED INPUT SWING
300
OUTPUT INVERTER
DIFFERENTIAL INPUT
HALF INPUT REPLICA
OPAMP
OUTPUT INVERTER REPLICA
OUT_N
OUT_P
INV0
INV1
INV2
VDD
VSS
vdd
vss
IN_P
IN_N
P0
P2
P5
P6
P8
N0
N2
N4
N6
N8
MP11
MP51
MP26
MN41
MN5
MN75
MP63
MP31
MN15
MN76
1P1V
1P1V_LVT
s1
s2
CTRL
Vthreshold
inv_bias
fb
OP_AMPout
in-
in+
-
+

FIG. 3

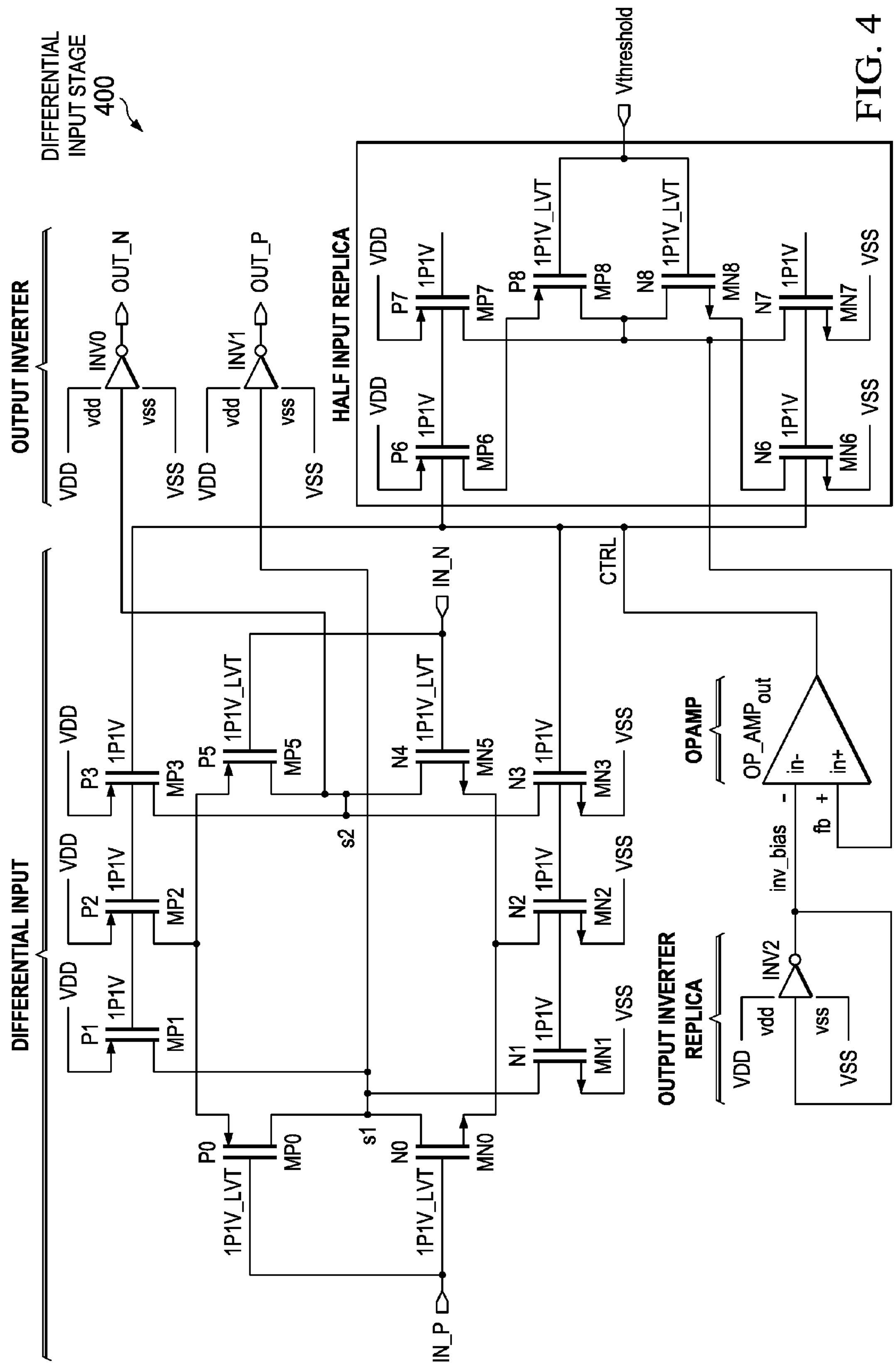

DIFFERENTIAL INPUT STAGE
400
OUTPUT INVERTER
DIFFERENTIAL INPUT
HALF INPUT REPLICA
OPAMP
OUTPUT INVERTER REPLICA
Vthreshold
OUT_N
OUT_P
INV0
INV1
INV2
IN_N
IN_P
CTRL
s1
s2
inv_bias
fb
OP_AMP_out
in-
in+
VDD
VSS
vdd
vss
P0
P1
P2
P3
P5
P6
P7
P8
N0
N1
N2
N3
N4
N6
N7
N8
MP0
MP1
MP2
MP3
MP5
MP6
MP7
MP8
MN0
MN1
MN2
MN3
MN5
MN6
MN7
MN8
1P1V
1P1V_LVT

FIG. 4

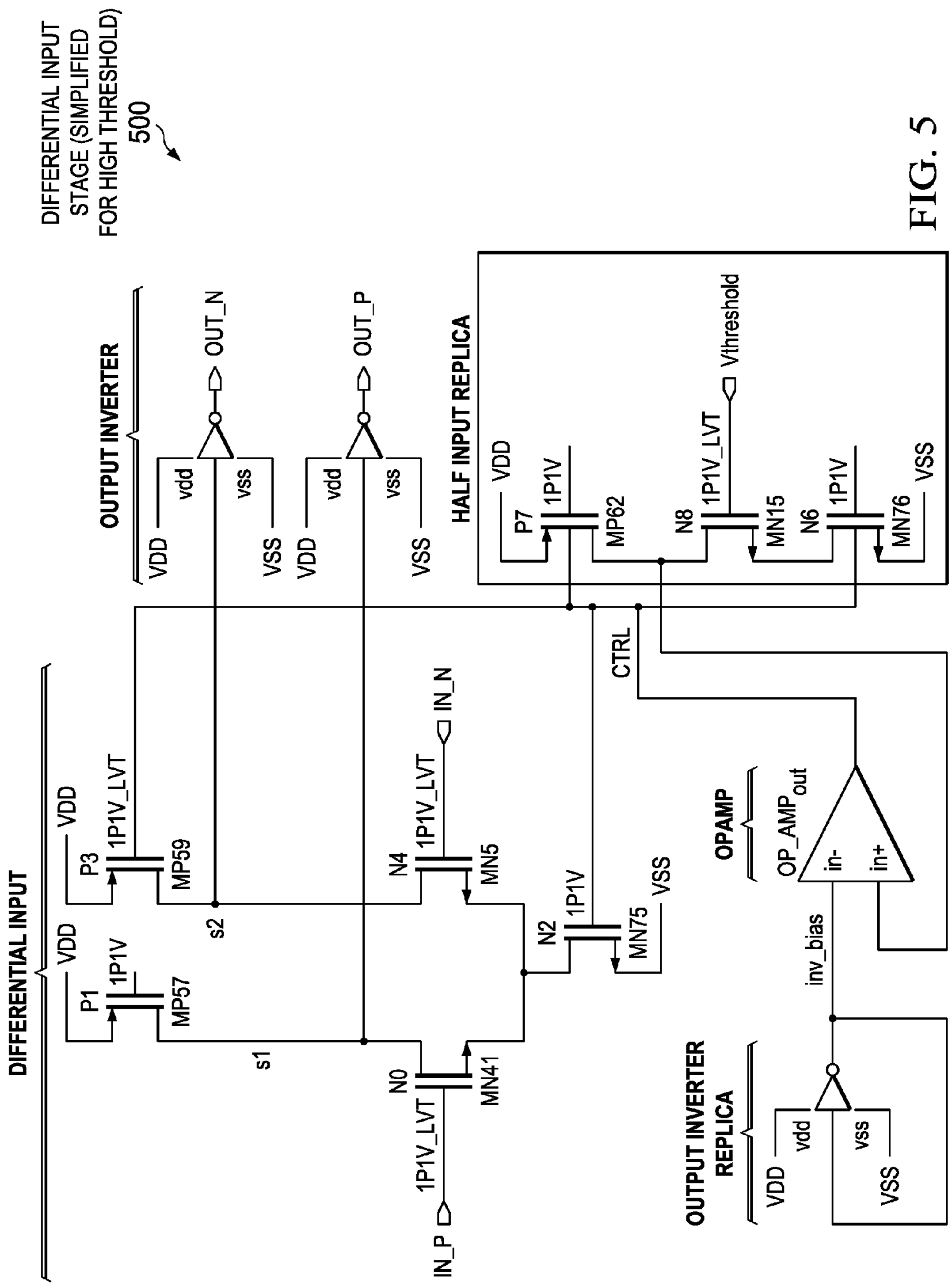

DIFFERENTIAL INPUT STAGE (SIMPLIFIED FOR HIGH THRESHOLD)
500
DIFFERENTIAL INPUT
OUTPUT INVERTER
HALF INPUT REPLICA
OPAMP
OUTPUT INVERTER REPLICA
VDD
VSS
vdd
vss
P1
P3
N0
N2
N4
P7
N8
N6
MP57
MP59
MN41
MN5
MN75
MP62
MN15
MN76
1P1V
1P1V_LVT
s1
s2
IN_P
IN_N
OUT_N
OUT_P
Vthreshold
CTRL
inv_bias
OP_AMP_out
in-
in+

FIG. 5

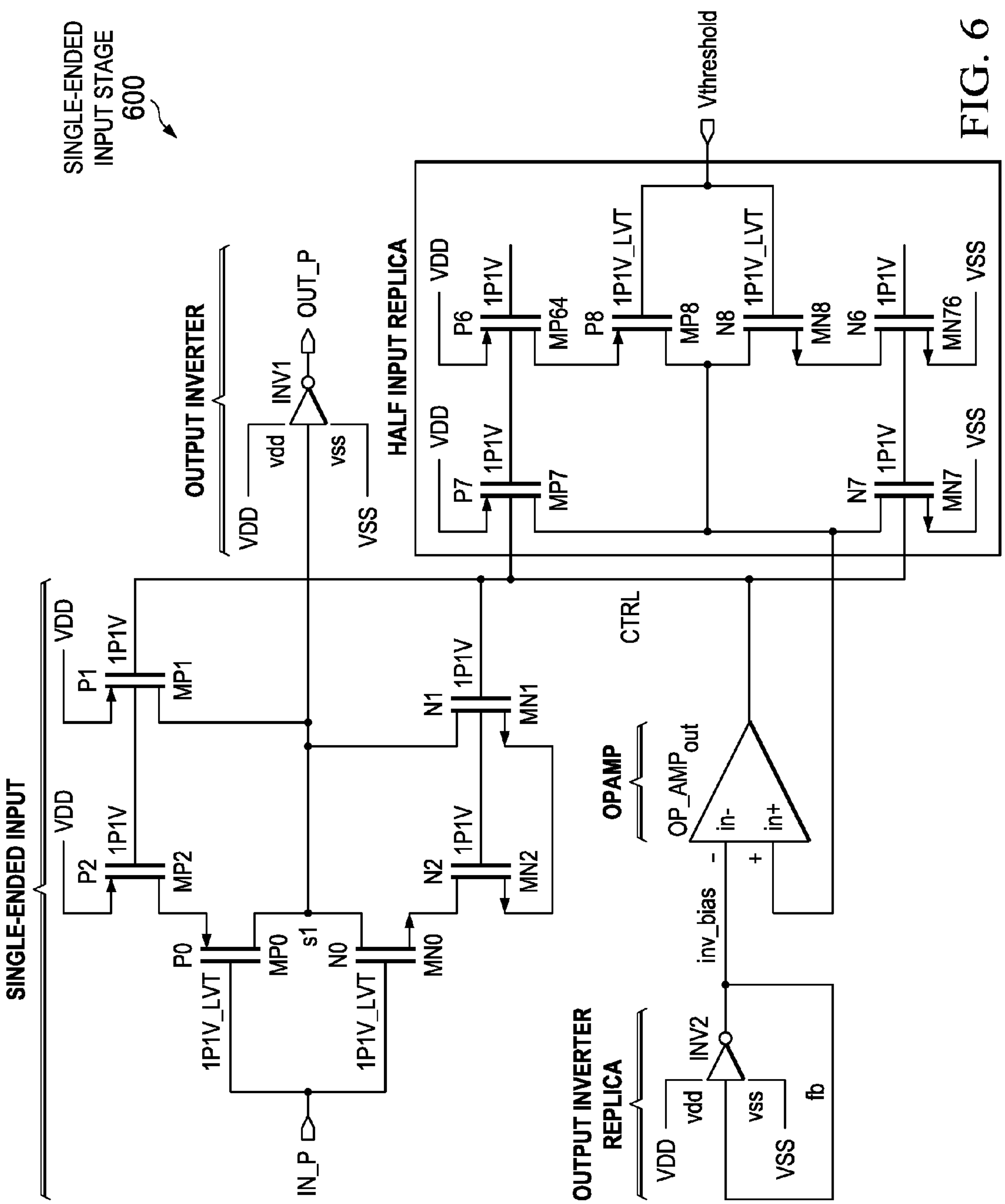

SINGLE-ENDED INPUT STAGE
600
SINGLE-ENDED INPUT
OUTPUT INVERTER
HALF INPUT REPLICA
OPAMP
OUTPUT INVERTER REPLICA
IN_P
OUT_P
Vthreshold
CTRL
inv_bias
OP_AMP_out
in-
in+
-
+
s1
fb
INV1
INV2
VDD
VSS
vdd
vss
P0
MP0
N0
MN0
P1
MP1
N1
MN1
P2
MP2
N2
MN2
P6
MP64
P7
MP7
P8
MP8
N8
MN8
N6
MN76
N7
MN7
1P1V
1P1V_LVT

FIG. 6

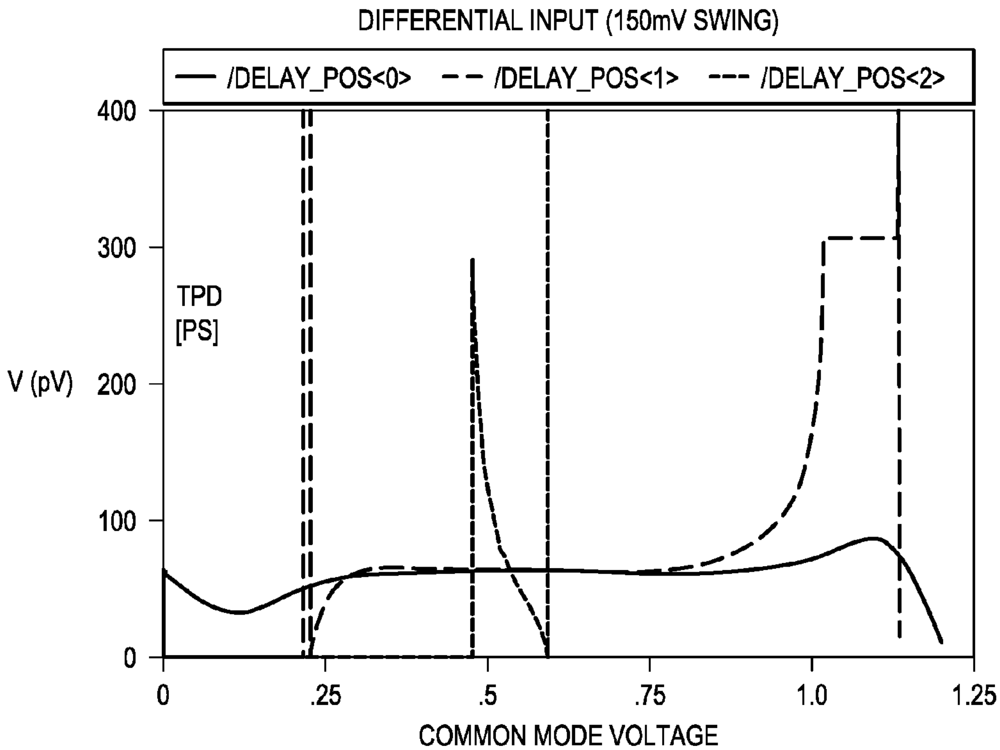

DIFFERENTIAL INPUT (150mV SWING)
/DELAY_POS<0>
/DELAY_POS<1>
/DELAY_POS<2>
TPD
[PS]
V (pV)
400
300
200
100
0
.25
.5
.75
1.0
1.25
COMMON MODE VOLTAGE

FIG. 7A

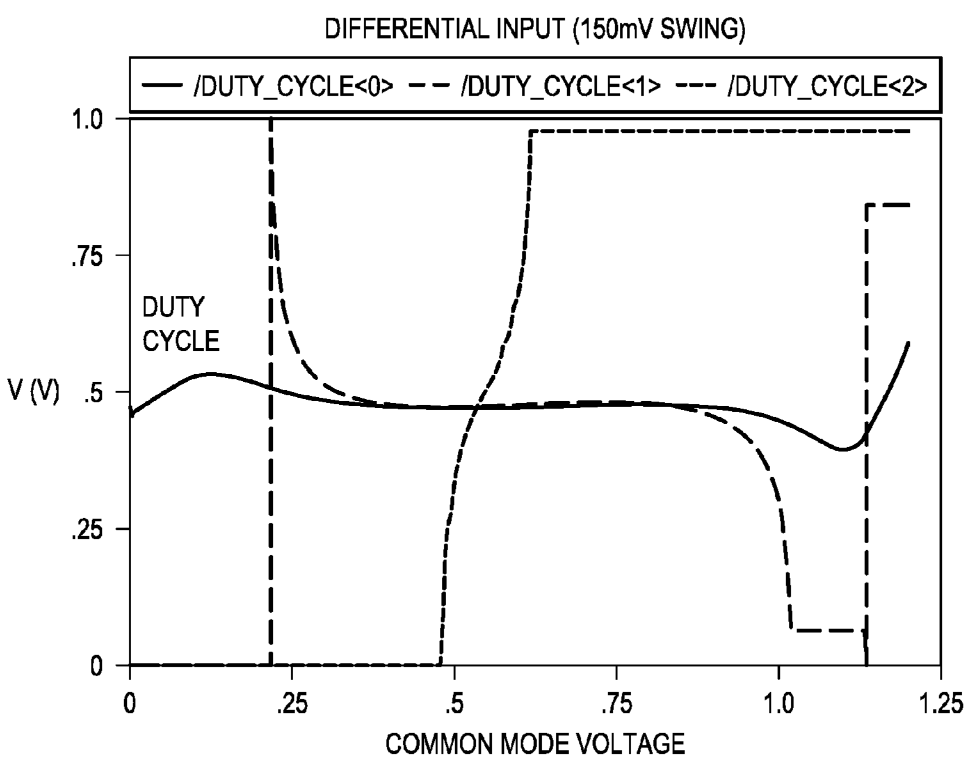

DIFFERENTIAL INPUT (150mV SWING)
/DUTY_CYCLE<0>
/DUTY_CYCLE<1>
/DUTY_CYCLE<2>
DUTY
CYCLE
V (V)
1.0
.75
.5
.25
0
.25
.5
.75
1.0
1.25
COMMON MODE VOLTAGE

FIG. 7B

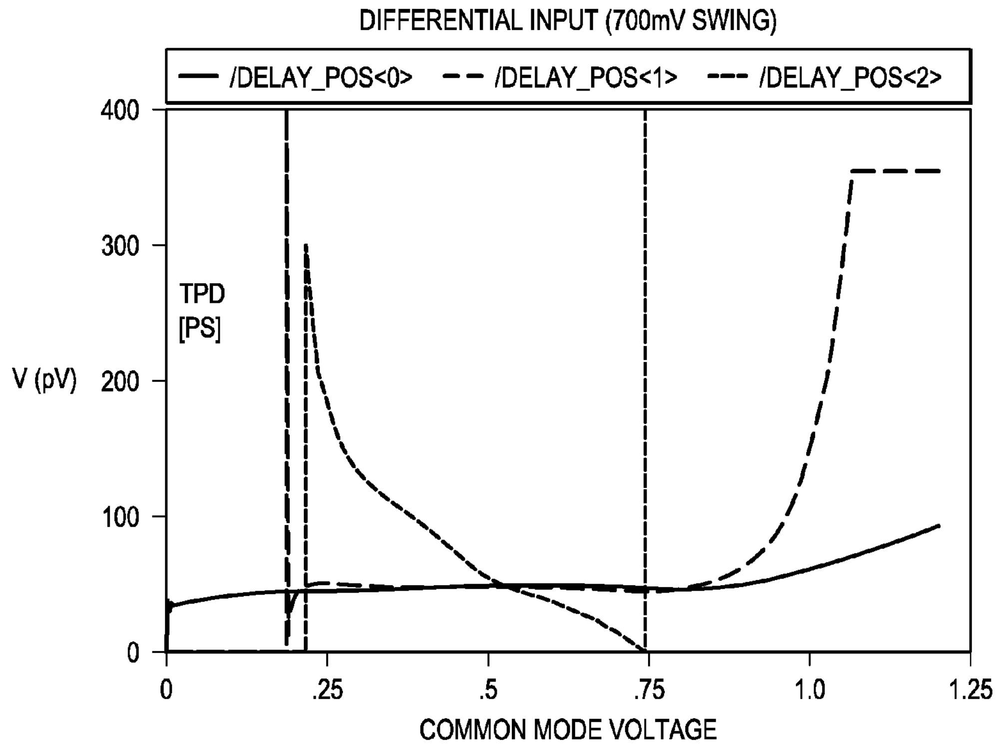

DIFFERENTIAL INPUT (700mV SWING)
/DELAY_POS<0>
/DELAY_POS<1>
/DELAY_POS<2>
TPD
[PS]
V (pV)
400
300
200
100
0
0
.25
.5
.75
1.0
1.25
COMMON MODE VOLTAGE

FIG. 7C

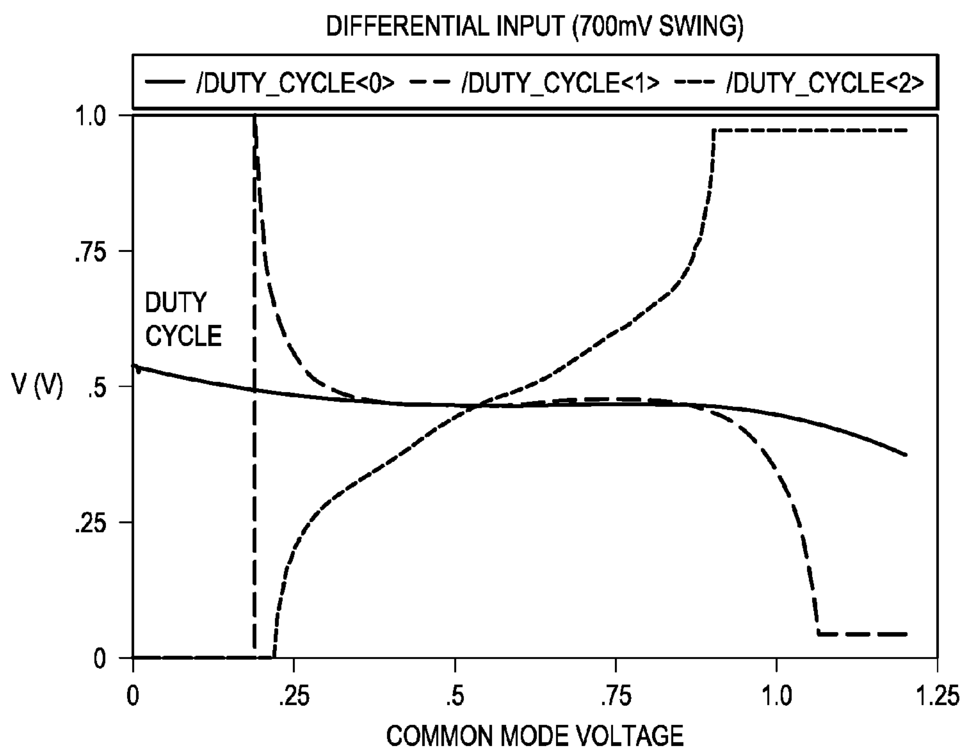

DIFFERENTIAL INPUT (700mV SWING)
/DUTY_CYCLE<0>
/DUTY_CYCLE<1>
/DUTY_CYCLE<2>
DUTY
CYCLE
V (V)
1.0
.75
.5
.25
0
0
.25
.5
.75
1.0
1.25
COMMON MODE VOLTAGE

FIG. 7D

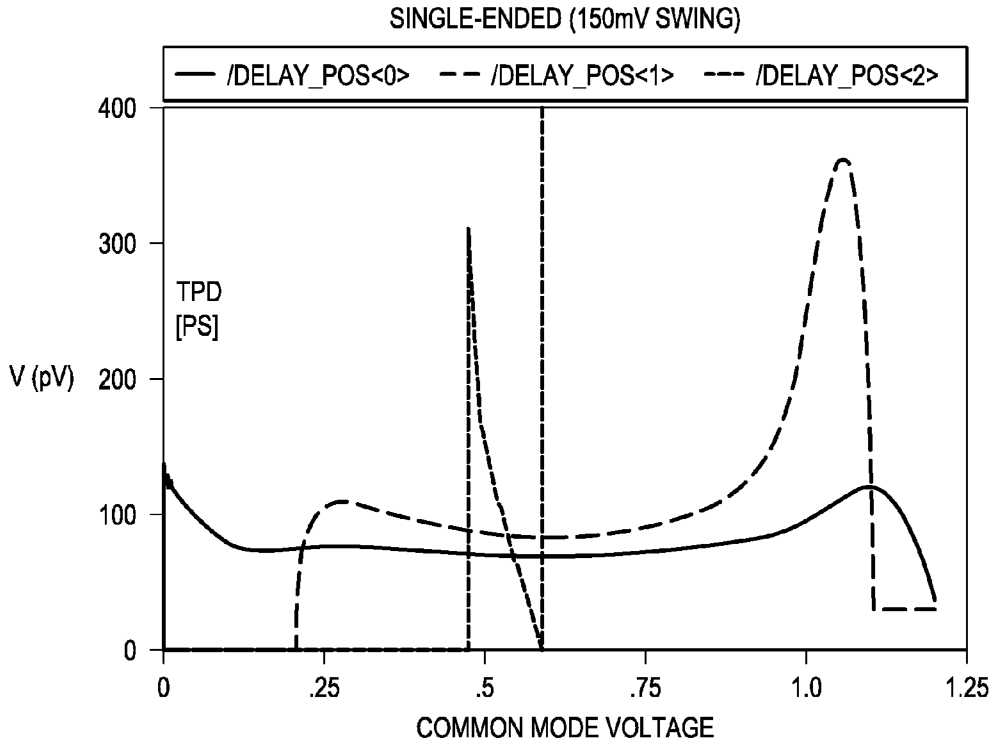

SINGLE-ENDED (150mV SWING)
/DELAY_POS<0>
/DELAY_POS<1>
/DELAY_POS<2>
400
300
200
100
0
TPD
[PS]
V (pV)
0
.25
.5
.75
1.0
1.25
COMMON MODE VOLTAGE

FIG. 7E

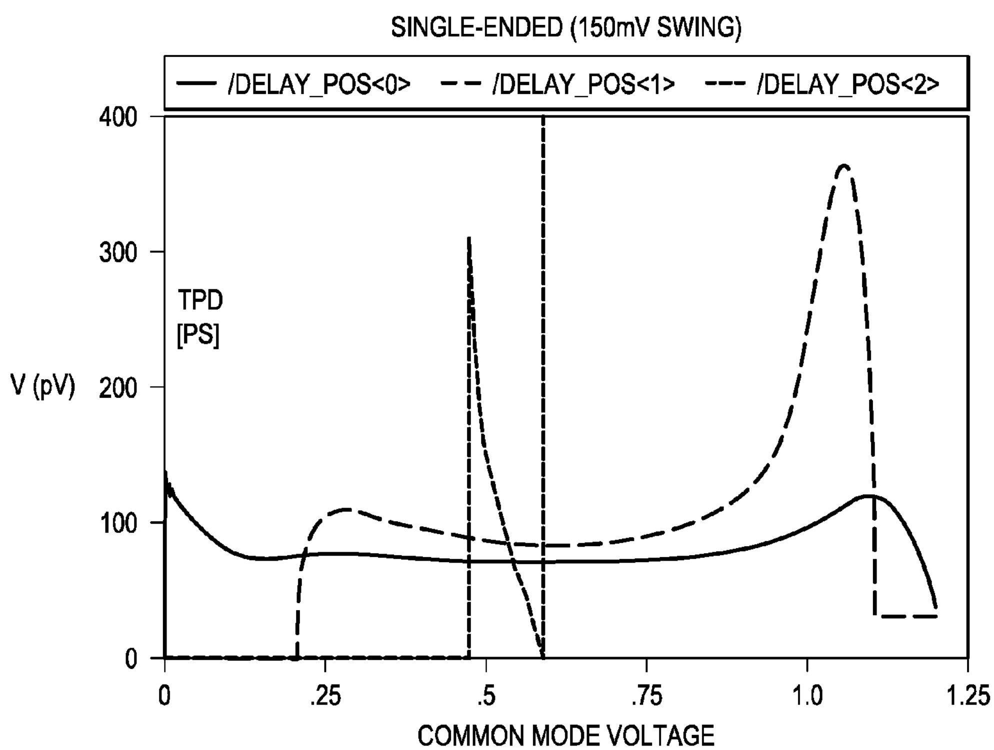

SINGLE-ENDED (150mV SWING)
/DELAY_POS<0>
/DELAY_POS<1>
/DELAY_POS<2>
400
300
200
100
0
TPD
[PS]
V (pV)
0
.25
.5
.75
1.0
1.25
COMMON MODE VOLTAGE

FIG. 7F

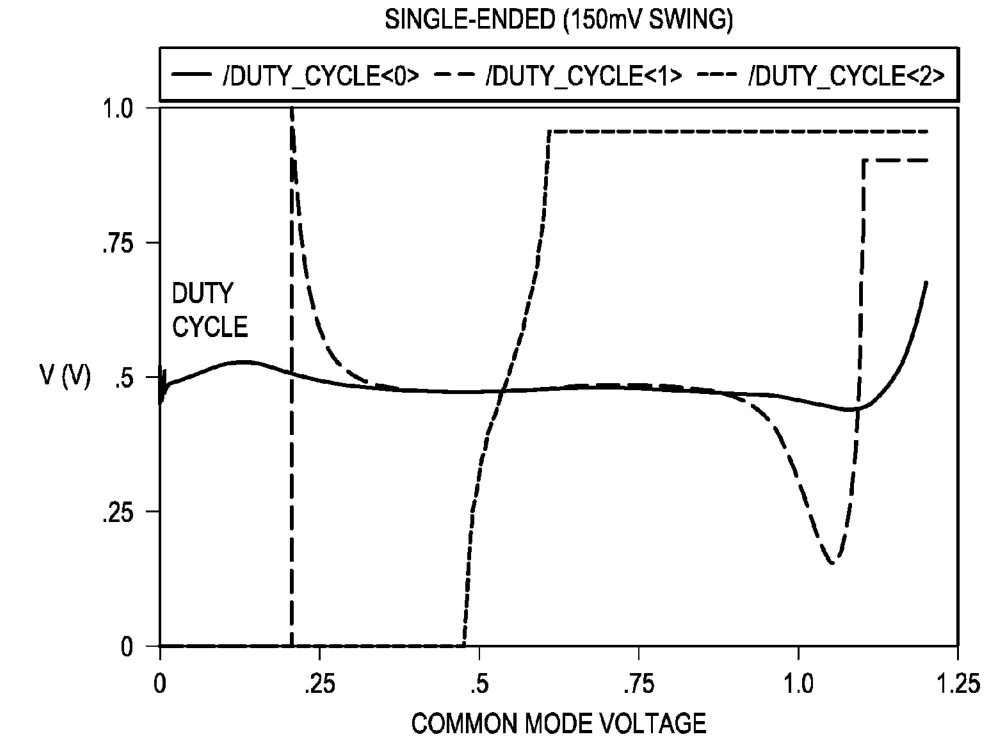

SINGLE-ENDED (150mV SWING)
/DUTY_CYCLE<0>
/DUTY_CYCLE<1>
/DUTY_CYCLE<2>
DUTY
CYCLE
V (V)
1.0
.75
.5
.25
0
0
.25
.5
.75
1.0
1.25
COMMON MODE VOLTAGE

FIG. 7G

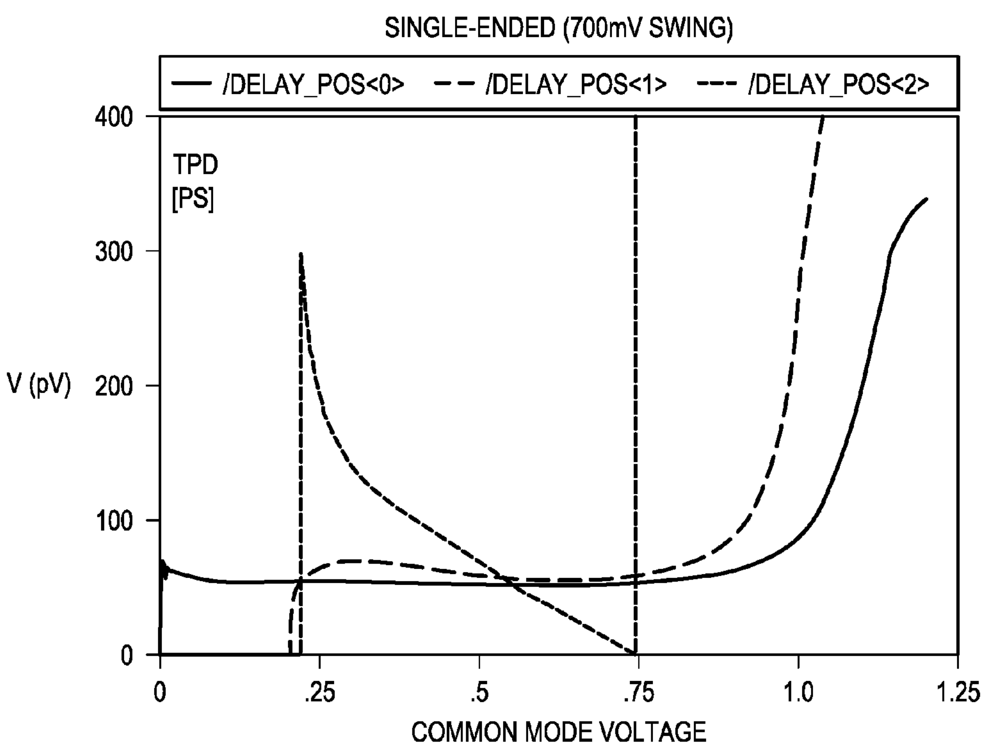

SINGLE-ENDED (700mV SWING)
/DELAY_POS<0>
/DELAY_POS<1>
/DELAY_POS<2>
TPD
[PS]
V (pV)
400
300
200
100
0
0
.25
.5
.75
1.0
1.25
COMMON MODE VOLTAGE

FIG. 7H

HIGH SPEED, RAIL-TO-RAIL CMOS DIFFERENTIAL INPUT STAGE

PRIORITY

This application claims the benefit of Provisional Application No. 61/993,943, filed May 15, 2014, entitled "High Speed, Rail-to-Rail CMOS Differential Input Stage," which is incorporated by reference in its entirety for all purposes.

TECHNICAL FIELD

This Application is directed, in general, to a rail to rail differential input stage and, more specifically, to a high speed, rail to rail CMOS differential input stage.

BACKGROUND

In high speed digital VLSI designs, input buffers comply with the (LV) TTL interface standard, which is good enough for most applications. These input buffers are simple CMOS inverter based receivers. However, when timing becomes critical, matching between differential clocks and data signal streams are important, input signals vary in swing and common mode, such buffers are not sufficient.

State of the art receivers are complex and their design is a compromise between high speed, input offset voltage, input common-mode range, power consumption, etc.

Wide input common-mode receivers are built-on NMOS/PMOS differential (complimentary) pair with folded cascode and with a common mode feedback amplifier. Such operational amplifiers are well described in the open literature. Normally, they do not reach high speed, consume a lot of power (especial in inactive mode) and require a settling time.

On the other hand are these very fast input receivers with a reduced input common mode voltage range, e.g. simple CMOS inverters operating in push-pull fashion, self-biased CMOS receivers.

Turning to FIG. **1**, illustrated is a prior art two-stage CMOS inverter based receiver. The input threshold, the output duty-cycle and the delay time changes a lot over process, supply and temperature (PVT) variations. Moreover, the duty-cycle and the delay time depend on the input signal amplitude and level. For most applications it's sufficient but moving on to higher speed, critical timings and low supply this basic stage cannot be used.

SUMMARY

A first aspect provides an apparatus, comprising: a differential input stage with signals IN_P & IN_N as input and OUT_P & OUT_N as output.

A second aspect provides an apparatus comprising: g: a single-ended input stage with signals IN_P & IN_N as input and OUT_P & OUT_N as output.

A third aspect provides an apparatus, comprising an apparatus, comprising a single-ended input stage with signals IN_P & IN_N as input and OUT_P & OUT_N as output, wherein the differential input controlled by transistors P**1**-**3** and N**1**-N**3**; and a means for weighting (sizing) of transistor (P**1** & P**3**) relative to P**2** and (N**1** & N**3**) relative to N**2** defines the optimal operation mode.

BRIEF DESCRIPTION OF THE DRAWINGS

Reference is now made to the following descriptions:

FIG. **1** illustrates a prior art input stage;

FIG. **2**A illustrates a single ended input stage with a limited input swing;

FIG. **2**B illustrates a second single-ended input stage with a limited input swing;

FIG. **3** illustrates a fully complementary configured rail to rail driver;

FIG. **4** illustrates another aspect of a rail to rail driver;

FIG. **5** illustrates an NMOS differential input pair with a PMOS current source load;

FIG. **6** illustrates an equivalent circuit for a single ended input; and

FIG. **7**A-illustrates a first simulation of the various above circuits;

FIG. **7**B illustrates a second simulation of the various above circuits;

FIG. **7**C illustrates a third simulation of the various above circuits;

FIG. **7**D illustrates a fourth simulation of the various above circuits;

FIG. **7**E illustrates a fifth simulation of the various above circuits;

FIG. **7**F illustrates a sixth simulation of the various above circuits;

FIG. **7**G illustrates a seventh simulation of the various above circuits;

FIG. **7**H illustrates an eight simulation of the various above circuits; and

FIG. **7**I illustrates a ninth simulation of the various above circuits.

DETAILED DESCRIPTION

Turning to FIG. **2**A, illustrated is a circuit **200** with a modification with decreased input threshold sensitivity is illustrated. A control loop set in input threshold to a predefined voltage (at pin 'Vthreshold'). Transistor P**2** and N**2** connects the input inverter to the supply and a replica of this inverter is connected to 'Vthreshold'.

For a given voltage at 'Vthreshold', the op-amp controls the output voltage of the inverter to be VDD/2 (set by the resistor divider). The gain of the second inverter 'INV**1**' could be optimized for VDD/2 when proper designed.

The characteristics of the input receiver described here are: high speed, wide input common mode range, constant small-signal and large-signal behavior, constant duty-cycle and a zero settling time.

The new input stage behaves like a very fast CMOS inverter based stage when the input signal has a high swing and the input common-mode voltage is in the middle. When the input signal swing is small and the input common-mode voltage becomes close to the power rails, it behaves like a NMOS or PMOS differential input pair with a current source load and at least with one differential pair alive. The transition from one to the other operation mode is smooth.

Typical applications are the DDR3/4 registers and data-buffers supporting high speed clocks and random data-pattern streams. Matched single-ended and differential receivers with variable reference voltages are required. Power consumption is a big concern and therefore a fast enabling/disabling of the receivers is desired.

Turning to FIG. **2**B, illustrated with employment of a second step, a reference voltage at the op-amp is set to the switching point of the driver (INV**1**) **201**. Inverter INV**2** is a replica of INV**1** and the output is shorted to the input. This self-biasing creates a negative-feedback and corrects any variations in processing parameters or operating conditions by shifting the biasing voltage away from their nominal values. Doing so, the duty-cycle will be improved and becomes independent on input swing and level. The control loop set the input threshold to 'Vthreshold' and biased the driver (INV**1**) to an adequate operation point. For a low input threshold, the op-amp switches the NMOS transistor N**6** and N**2** to a stronger drive value and the PMOS transistor P**6** and P**2** to a weaker drive value. For a high input threshold, the other way around. The same mechanism applies to PVT variations.

Regarding FIG. **3**, a same principle can be used for differential input signals of an inverter **300**. The inverter **300** is a fully complementary configured rail to rail driver. The biasing is accomplished through transistor P**2** and N**2**. They are operating in the linear region and their source voltages are close to the supply rails. The output voltage swing will be rail-to-rail and the interface to the CMOS level becomes straight-forward therefore. The complementary structure leads to doubling the dc gain of the stage. For the input threshold and duty-cycle the same rules apply as describe above. The inverter circuit **300** works best when 'Vthreshold' tracks the input common mode voltage.

This is normally done by the employment of a common mode feedback circuit (CMFB). CMFB loops require a settling time and therefore would limit the applications for receivers with uninterrupted clock signals only. For applications where the incoming clock could be enabled/disabled or the data signal is a random data pattern, CMFB loops are not suitable. The describe circuit here requires a predefined common mode voltage.

This input stage has a limited input common mode range. When the input voltage falls below 'Vt_NMOS' or rise about 'VDD-Vt_PMOS', the circuit operates very weak or does not work anymore. Assuming both inputs are low, the transistors N**0** and N**4** are completely switched off. There is nothing that can pull node 's**1**' and 's**2**' to ground. For both inputs are high it's the other way around.

Turning to FIG. **4**, only a few components are needed to widen the input common mode range as shown for a rail to rail driver **400**. Current source loads (P**1**/N**1**, P**3**/N**3**) are added to node 's**1**' and node 's**2**' respectively. The same is done in the half replica circuit. They are connected to the same control voltage (CRTL) and are part of the control loop. Assuming the input common mode voltage is at a high level, such that the PMOS differential input pair is switched off.

Turning to FIG. **5**, the remaining, active circuit **500** is shown. It is a NMOS differential input pair with a PMOS current source load. A complementary picture can be drawn in case of a low level input common mode voltage.

The impact of each circuit part (operation like shown in FIG. **3** or more like shown in FIG. **5**) depends on the input common mode level and the sizing of the transistors. The transition from one to the other mode is smoothly and overlapping.

Turning to FIG. **6**, an equal circuit can be designed for single-ended input. **600**.

Turning to FIGS. **7**A, **7**B, **7**C, **7**D, **7**E, **7**F, **7**G, **7**H, and **7**I, simulations have been done for single-ended and differential input signals and for 150 mV and 700 mV signal swing (see pictures at the end of this paper). The supply voltage is 1.2V and the input common mode voltage has been ramped from 0V to 1.2V (on the x-axis). On the y-axis, the duty-cycle and propagation delay time (input to output) is shown. The result is shown for circuit of FIG. **1** (dotted, blue), FIG. **3** (dashed, blue) and FIG. **4** (solid, red).

Notable is the constant propagation delay time and duty-cycle over a wide input common mode range of the new circuit (FIG. **4**). For critical timings the dependency upon input signal shapes (data and/or clock-signal) is canceled out almost.

Those skilled in the art to which this application relates will appreciate that other and further additions, deletions, substitutions and modifications may be made to the described embodiments.

What is claimed is:

1. An apparatus, comprising:

a differential input stage to receive input signals IN_P and IN_N and provide output signals OUT_P and OUT_N;

the differential input stage including

a first differential input PMOS/NMOS transistor pair to receive IN_P, and to generate an inverted IN_P at a differential output node S**1**, which is coupled to an output inverter INV**1** to generate OUT_P;

a second differential input PMOS/NMOS transistor pair to receive IN_N, and to generate an inverted IN_N at a differential output node S**2**, which is coupled to an output inverter INV**0** to generate OUT_N; and

a bias network to implement a common mode control loop to generate a bias control voltage, and including

a high bias PMOS transistor coupled between a high rail and respective PMOS transistors of the first and second PMOS/NMOS transistor pairs, and to receive the bias control voltage;

a low bias NMOS transistor coupled between a low rail and respective NMOS transistors of the first and second PMOS/NMOS transistor pairs, and to receive the bias control voltage;

a common mode control circuit including

a half-replica PMOS/NMOS transistor pair that is a replica of a selected one of the first and second differential input PMOS/NMOS transistor pairs, to receive a common mode control voltage Vthreshold, and to generate an inverted Vthreshold voltage at a Vthreshold node;

a replica high bias PMOS transistor and a replica low bias NMOS transistor that are respectively a replica of the high bias PMOS and low bias NMOS transistors, coupled respectively between the high rail and the replica PMOS transistor, and the low rail and the replica NMOS transistor, to receive the bias control voltage;

a replica output inverter that is a replica of a respective one of the output inverter INV**1** and output inverter INV**0**, with an output shorted to an input; and

an amplifier to receive at a non-inverting input the inverted Vthreshold voltage, and at an inverting input an output of the replica output inverter, and to generate the bias control voltage; and

the differential input stage further including common mode range control circuitry including

a third PMOS/NMOS transistor pair to provide a first current source load, with PMOS and NMOS transistors coupled respectively between the high and low rails and the differential output node S**1**;

a fourth PMOS/NMOS transistor pair to provide a second current source load, with PMOS and NMOS transistors coupled respectively between the high and low rails and the differential output node S**2**; and

a replica PMOS/NMOS transistor pair to provide a replica current source load that is a replica of a selected one of the first and second current source loads, with PMOS and NMOS transistors coupled respectively between the high/low rail and the Vthreshold node.

2. The apparatus of claim **1**, wherein the respective PMOS and NMOS transistors of the first and second current source loads are sized respectively relative to the high bias PMOS and low bias NMOS transistors for an optimal operation mode.

3. The apparatus of claim **1**, wherein the amplifier comprises an operational amplifier.

4. The apparatus of claim **1**, wherein the propagation delay time through the differential input stage relative to common mode voltage is substantially constant.

5. The apparatus of claim **1**, wherein the duty-cycle of the differential input stage relative to common mode voltage is substantially constant.

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